PROTEUS

DESIGN SUITE

www.labcenter.com

Product Guide

Electronics Design

From Concept

To Completion

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Electronics

The Proteus Design Suite combines schematic capture, SPICE circuit simulation, and PCB design to make a complete electronics design system. Add to that the ability to simulate popular micro-controllers running your actual firmware, and you have a package that can dramatically reduce your development time when compared with a traditional embedded design process.

System Features & Benefits

System Components

- ISIS Schematic Capture - an easy to use yet extremely powerful tool for entering your designs.

- PROSPICE Mixed mode SPICE simulation - industry standard SPICE3F5 simulator combined with high speed digital simulator.

- ARES PCB Layout - high performance PCB design system with automatic component placer, rip-up and retry auto-router and interactive design rule checking.

- VSM - Virtual System Modelling lets you co-simulate embedded software for popular micro-controllers alongside your hardware design.

System Benefits

- Integrated package with common user interface and fully context sensitive help make for a quick and easy learning process.

- Technical support direct from the program authors means that expert help is available when you need it.

- Virtual Prototyping with Proteus VSM substantially cuts both software and hardware development time and cost.

Company Profile

Labcenter Electronics Ltd. was founded in 1988 by chairman and chief software architect John Jameson. The initial launch of the Proteus Design Suite followed soon after and has since benefited from over 18 years continuous development, evolving into one of the most cost effective, fully featured EDA packages on the market. With current sales in over 50 countries spanning the globe Labcenter is continuously expanding both its product portfolio and its customer base.

Our goal is to provide you, the customer, with the best package at the best price. To achieve this our company focus is threefold :

Product Innovation

When deciding development strategies we focus on usefulness, timesaving capabilities and customer feedback. We introduced the world to complete embedded software co-simulation with Proteus VSM (and are still a world leader in the field) as well as numerous features across the Proteus suite that have subsequently percolated through to competitive offerings.

Since its inception Labcenter has increased its R&D budget annually (indeed, almost exponentially in recent years!) - product innovation backed by a world class software development team is one of our primary strengths and has allowed Proteus to grow into a truly complete CAD system.

Continuous Development

Unlike some packages on the market today our policy is, and always has been, one of continuous development on features that reduce the time to market for our customers. Typically, we release three to four versions per year with major functional enhancements in addition to maintenance and minor releases as required. This focus on development makes us more dynamic as a company and allows us the flexibility to provide both new functionality and maintenance releases to the customer more frequently.
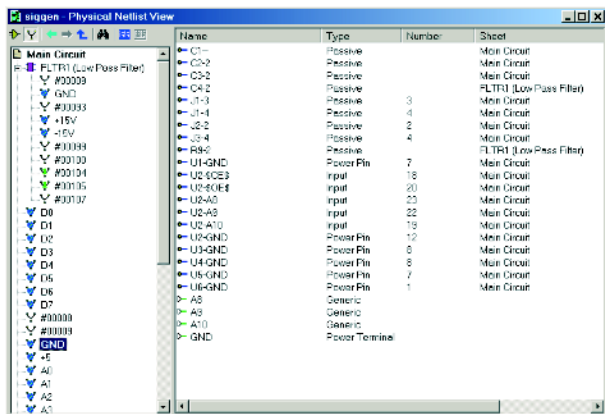
Customer Care

We believe that customer care is a keystone of our success. Our technical support is free both via telephone and email for professional users and our support staff are all experienced users of the software. Direct channels exist to the development team allowing us to provide quick and comprehensive responses to even the most complex problems. We consider user feedback to be of vital importance when determining development schedules for new releases and have a formal system for logging and prioritising implementation of such features.

Integrated Package

The Proteus Design Suite comprises a fully integrated EDA package with modules for schematic capture (ISIS), circuit simulation (PROSPICE), PCB layout (ARES) and embedded co-simulation (VSM). The simulation functions take place entirely within the schematic editor whilst ISIS and ARES share a common, easy to use, Windows user interface. All of which reduces the time it will take you to master the software.

Naturally, ISIS and ARES are themselves tightly integrated, offering both forward and backward annotation and a unique Design Explorer which allows you to navigate and cross probe between the schematic, netlist and PCB databases.

Modern User Interface

Much of the power of an application can be lost on its users if is difficult to learn, or hard to use. On the one hand, newcomers to the package will give up if they cannot manage to produce something fairly quickly whilst on the other hand, expert users tend to become frustrated if they cannot do the things they have to do often as quickly and easily as possible.

In Proteus, we have addressed the first issue by making the editors work very much like the standard Windows applications that every computer literate user is already familiar with. In addition, detailed, graphical tutorials help the newcomer become productive as quickly as possible.

Meanwhile, the expert user will soon appreciate that the editors are largely modeless. Objects can be placed, wired, moved, edited and deleted without having to switch between several different modes.

Finally, all users - beginner and expert alike - will appreciate that detailed context sensitive help is never more than a mouse click away, whilst expert technical help is no more than a phone call away.
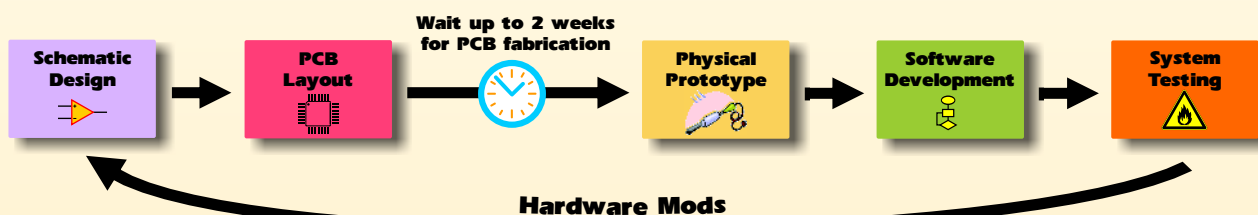
The VSM Advantage

The Proteus Design Suite is wholly unique in offering the ability to co-simulate both high and low-level micro-controller code in the context of a mixed mode SPICE circuit simulation. With this Virtual System Modelling facility, you can transform your product design cycle, reaping huge rewards in terms of reduced time to market and lower cost of development.

If one person designs both the hardware and software, then that person benefits because the hardware design may be changed just as easily as the software design. In larger organizations where the two roles are separated, the software designers can begin work as soon as the hardware team have a produced a schematic; there is no need for them to wait until a physical prototype exists.

This is the 'VSM Advantage'.

The VSM Advantage

With traditional design tools, software development and system testing cannot begin until a PCB and physical prototype are available - incurring a delay of up to 2-3 weeks. And if something is wrong with the hardware design, the whole process must be repeated.

Using Proteus VSM, software development can begin as soon as the schematic is drawn, and the combination of hardware and software can be thoroughly tested before physical prototyping.

ISIS Intelligent Schematic Input System

ISIS lies right at the heart of the PROTEUS system and is far more than just another schematics package. It combines an exceptionally powerful design environment with the ability to control most aspects of the drawing appearance. Whether your requirement is the rapid entry of complex designs for simulation & PCB layout, or the creation of attractive schematics for publication, ISIS is the tool for the job.
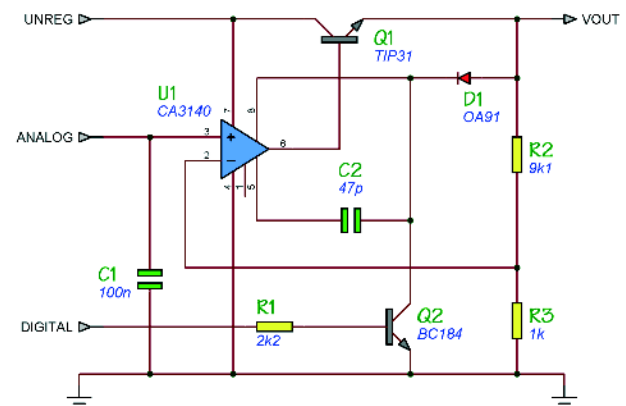
Schematic Capture

Features

- Produces publication quality schematics.

- Style templates allow customization of supplied library parts.

- Mouse driven, context sensitive user interface.

- Automatic 'follow me' wire routing and junction dot placement/removal.

- Hierarchical design including parameterization of sub-circuit component values.

- Full support for buses including sub-circuit ports and bus pins.

- Preview of PCB footprints whilst selecting components and making new library parts.

- Comprehensive representation for homogenous and heterogeneous multi-element parts including connectors.

- Sophisticated management of component properties including customization of the relevant dialogue forms.

- Large and growing component library of over 10,000 parts, most complete with ready to use simulator models.

- Netlist formats: Labcenter SDF, SPICE, SPICE-AGE, Tango, Boardmaker, EEDesigner, Futurenet, Racal & Valid.

- Electrical Rules Check and Bill of Materials reports.

- Output to any Windows printer device in colour or monochrome.

- Graphical export in WMF, BMP, DXF, EPS and HPGL formats.

Publication Quality Schematics

ISIS provides you with full control of the drawing appearance in terms of line widths, fill styles, colours and fonts. This enables you to produce attractive schematics like you see in the magazines rather than the 'thin line' diagrams often associated with older CAD software. Once your drawing is complete you can export it as a graphics file or copy it to the clipboard for incorporation in other documents. This makes ISIS ideal for use in producing technical documentation, academic papers, project reports, as well as being an excellent front end for PCB design.

The drawing appearance is defined in terms of a style template - especially useful if you want to apply a 'house style' to all your designs. Furthermore, the scheme allows you to customize the appearance of the library parts supplied with the package.

Context Sensitive User Interface

Much thought has gone into making the most common drawing operations as quick and easy as possible. In particular, ISIS has no wiring mode per se. Instead, you can place a wire at any time by clicking on a component pin or on a previously placed wire. In addition, place, edit, move and delete operations can be achieved directly with the mouse, without having to go through menus or icons.

This makes ISIS very quick to use indeed**.**

Wire Auto-Router

Placing a wire can be as simple as clicking on the two pins you want to connect - the Wire Auto-Router does the rest. But if you want a wire in a particular place, you can just click at the intermediate corners. The Wire Auto-Router also operates when components are moved, automatically fixing up the affecting wiring.

Junction dots are placed and removed automatically. As well as saving time, this avoids ambiguities that might otherwise arise. Manual placement of dots is also allowed, should you prefer to place a dot and then wire to it.

Hierarchical Design

As well as supporting normal multi-sheet designs (equivalent to a circuit spread over several pieces of paper), ISIS supports hierarchy within a design. In other words, a particular component can be defined as a module which is then represented by a further circuit diagram. The hierarchy can be nested to an arbitrary number of levels, and modules can be drawn as standard components, or as special sub-circuit blocks on which the interface ports can be placed and removed on the fly.
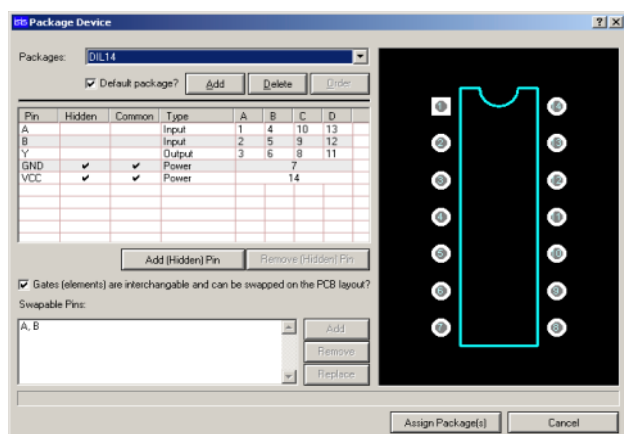
Full Support for Buses

Buses are used to represent multiple parallel connections, typically for data or address lines in microprocessor designs. ISIS provides not only a bus wire, but also the ability to define components and sub-circuits with bus pins. Therefore, a 32 bit processor bus connection between processor and memory can be represented as a single wire, saving both drawing time and space on the diagram.

Device Libraries

ISIS comes with a device library including over 10,000 parts. The libraries include standard symbols, transistors, diodes, thermionic valves, TTL, CMOS, ECL, microprocessor and memory parts, PLDs, analog ICs and op-amps as well as manufacturer specific libraries from National Semiconductor, Philips, Motorola, Teccor, Texas and Zetex. More libraries are being created as part of an ongoing programme.

Visual Packaging Tool

Matching schematic and PCB library parts is greatly simplified by the packaging tool. This displays the PCB footprint alongside the pins of the schematic part and allows both textual and graphical entry of pin numbers for each pin name.

Multi-Element Parts

The way in which ISIS represents library parts allows for all the common possibilities: single element (e.g. 555 timer), homogenous multi-element (four 7400 gates), and heterogenous multi-element (relay coil and contacts).
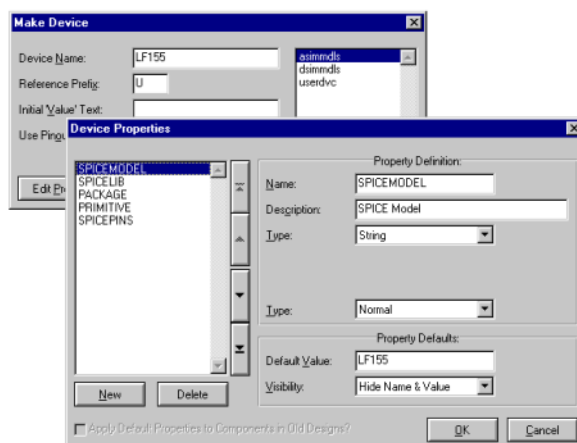
Gate elements are allocated automatically as you place components, and can be changed subsequently either by manual editing or through back-annotation from ARES.

Connectors can also be represented as individual pin elements such that they can be distributed across the schematic, rather than having to wire everything back to a single part.

Component Properties

Each component in your design can have an arbitrary number of properties or attributes. Some properties control specific functions of the software (e.g. PCB package, or simulator model) but you can also add your own properties to hold other information such as stock codes or component costs.

Furthermore, when a library part is created, default values and 'Property Definitions' can be supplied. Property definitions provide a plain English description of the property and cause it to be displayed in its own editing field when the component is edited. You can even specify appropriate range limits for numeric values, and keyword lists for strings. A special type for PCB packages allows for browsing of the ARES libraries.

Report Generation

ISIS supports many 3rd party netlist formats making it suitable as a front end for use with other software.

The Bill of Materials report can be configured to include whichever component properties you wish, and can also include column totals for selected numeric properties.

Equally useful is the ERC report which lists possible wiring mistakes such as unconnected inputs, conflicting outputs and mis-typed net-labels.

"We use the Proteus suite regularly and we really appreciate both the simple user interface and the number of features. When we have faced a limit or a problem, the support response has always been fast and focused. Proteus is a good solution for reasonably complex design."

Gael Salles - ST MicroElectronics

Interactive Mixed Mode Circuit Simulator

PROSPICE is a state of the art mixed mode circuit simulator that operates in conjunction with the ISIS schematic capture environment. Based around the industry standard SPICE3F5 analogue kernel, with our own extensions for mixed mode simulation and interactive circuit animation, PROSPICE provides a powerful, interactive environment in which to develop and test your designs.

Circuit Simulation

System Features

- Fully integrated with schematic capture environment.
- Supports both Graph Based and Interactive Circuit Simulation.
- Simulation Advisor helps with locating problems in the design or simulation.
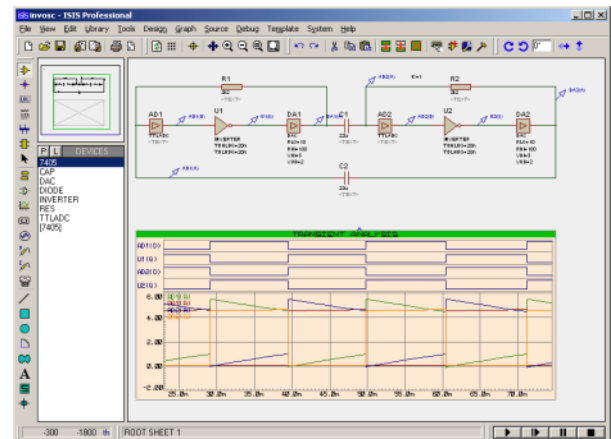
Analogue Simulation

- Genuine Berkeley SPICE3F5 analogue simulator kernel with extensions for true mixed mode operation.
- Graph Based Analyses: Operating Point, Transient, Frequency, DC Transfer Curve, DC Parameter Sweep, AC Parameter Sweep, Noise, Distortion, and Fourier, Input & Output Impedance.
- Advanced primitives include MOSFET Level 3, BSIM version 3, MESFET, lossy transmission line and expression based arbitrary source.
- Direct compatibility with manufacturers' SPICE models.
- Over 8000 models supplied with the package.

Digital Simulation

- Event driven digital simulation models timing, glitch and floating input behaviour.
- Fusemap models allow simulation of PLDs directly from JEDEC files.
- Full set TTL and CMOS models complete with timing information.
- Conformance analysis facilitates automatic testing of embedded systems.

Fully Integrated Environment

Circuit simulation within PROTEUS is conducted entirely from within the ISIS schematic capture module. Graphs appear alongside the components on the schematic, with circuit stimuli (generators) and probes being placed directly on the wiring. The circuit can be simulated at any time by pressing the space bar, making the edit-simulate cycle extremely rapid - far more so than in packages where the simulator is a separate application.

Graph Based or Interactive Simulation

In addition to traditional graph based circuit simulation, PROSPICE offers fully interactive circuit animation. You can control your design using mouse operated component models (e.g. switches, pots) and observe what is happening from on screen indicators (e.g. LEDs, 7 seg. displays, meters). Uniquely, it is possible to design your own actuators and indicators, making the system suitable for modelling the actual peripherals of a real design.

Additionally, numerous virtual instruments are provided including an Oscilloscope, a Logic Analyser, a Signal Generator, and Digital Pattern Generator. These operate in much the same way as their real world counterparts, making for a very intuitive approach to circuit simulation.

Simulation Advisor

Whether you are running a graph based or interactive simulation, PROSPICE records any problems with the design (e.g. logic contentions) or the simulation (convergence failure) to a log file. The messages are colour coded for severity and you can navigate to any related component or net on the schematic. Better still, there is help available for simulation error messages enabling you to understand and fix the cause of simulation failures as quickly as possible.

Partial Simulation of Large Designs

Where PROTEUS is being used to enter an entire design for PCB layout, it may be inappropriate to run simulation experiments on the entire schematic. For example, it does not usually make sense to simulate crystal oscillators as analogue circuits when testing the digital logic that they drive. PROSPICE saves you from carving up the schematic by supporting partial simulation of the design. The circuit topology is analysed and only those components located between the input stimuli and the measurement points are included in the simulation.
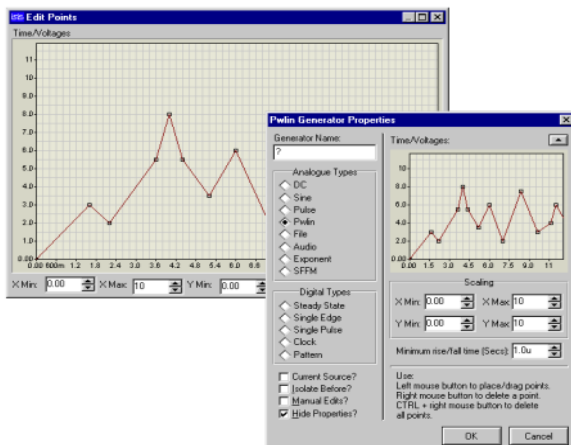
Excellent Modelling Tools

If you need to create your own component models, PROTEUS provides an excellent environment in which to do so. The support for hierarchical design in ISIS enables you to create a virtual test jig in which the component model can be developed. This means that any changes to the model can be evaluated quickly and easily prior to storing the model as a pre-compiled netlist.

PROSPICE also comes complete with a comprehensive set of primitives (i.e. building blocks) with which to construct your own models, whilst a DLL based API is also available for really complex modelling tasks.

SPICE3F5 Simulator Kernel

PROSPICE is based around the industry standard SPICE3F5 analogue simulator developed at Berkeley University, California.

It contains the latest convergence techniques and primitive models. PROSPICE uses Berkeley's source code wherever possible, guaranteeing best possible compatibility both in terms of numerical results, and support for manufacturers' SPICE models.
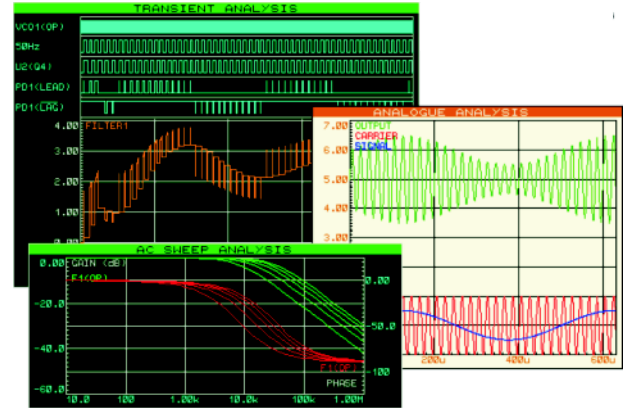
True Mixed Mode Simulation

PROSPICE incorporates extensions to standard SPICE which allow it to model digital circuitry using an event driven paradigm. This is much more efficient than attempting to model the transistor level behaviour. The combination of SPICE3F5 and our own digital simulator substantially outperforms XSPICE based systems, allowing many interactive simulations to run in real time.

Fully Compatible with Manufacturers' Models

More and more component manufacturers are providing SPICE models for their wares as well as the traditional data books. By choosing PROSPICE you will be able to gain maximum benefit from this resource - we have made a

point of using Berkeley code to parse the SPICE netlists in order to guarantee best possible compatibility. And to get you started, we have gathered over 5000 SPICE models from the Internet and linked them to appropriate schematic symbols in ISIS. A further 3000 of our own models make up a total of over 8000 models supplied with the package.

Feature Rich Digital Simulation

PROSPICE incorporates a fully featured event driven digital simulator which is automatically invoked whenever digital components are present. The digital simulation paradigm correctly models timing, glitch behaviour, floating inputs and undefined states - beware that not all so called mixed mode simulators are anything like as good.

PLD Modelling

PROSPICE includes special digital primitives which represent PLD fusemaps. These devices can be used to construct models of *any* programmable logic device. Specific models for popular PLD devices are included in the supplied component libraries.

The information on how the device is programmed is read directly from the JEDEC file produced by your PLD assembler. Therefore, you are not tied to using any particular PLD development system.

Conformance Analysis

This unique feature compares a new set of simulation results against reference data at pre-determined sampling points. Coupled with VSM co-simulations of embedded software, it becomes an extremely powerful quality assurance tool; changes to the hardware or software can be checked for unwanted side effects entirely automatically.

"After review of all available simulation packages, the performance power and capability of the Labcenter Proteus suite have proved invaluable to our cycle time on design of prototypes. Highly recommended for both professional and educational use, providing a cost effective solution to complex problems."

Tony Beddard - Vice President - Accent Optical Technologies

Proteus VSM is a unique family of products for co-simulation of microprocessor based designs. The simulated micro-controller chip runs your firmware just as in real life, and you can interact with it using a large range of peripheral models and powerful debugging tools. Proteus VSM is available for a number of popular micro-controller families. Each VSM package includes a copy of ISIS for schematic capture and a true mixed mode interactive simulation engine based on ProSPICE. Traditional graph based simulation is also available as an optional extra.

Micro-controller Co-Simulation

Features

- True co-simulation of CPU and analog/digital electronics.
- Extensive built in debugging facilities including register and memory contents, breakpoints and single stepping.
- Watch window and watchpoint expression breakpoints.
- Source level 'C', BASIC and assembly debugging supported for selected development tools.
- Multi CPU designs no problem.
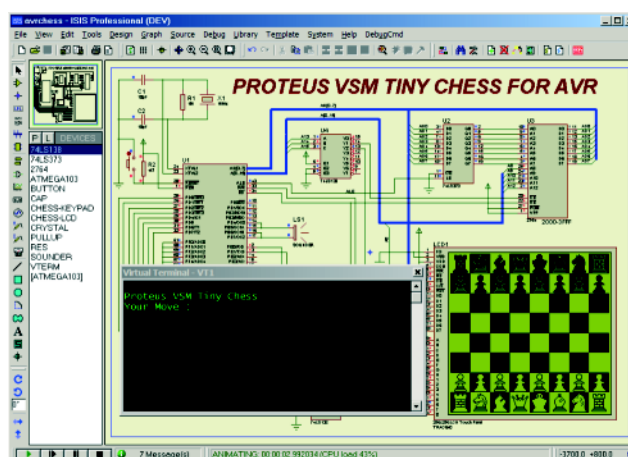
Supported CPU Families

- Microchip PIC12, PIC16, PIC18 and PIC24.
- 8051/8052 including Philips and Atmel variants
- AVR, Tiny AVR and Mega AVR
- ARM7 / Philips LPC2000.
- Motorola Freescale HC11 and Parallax BASIC Stamp.
- More models always under development.

Benefits

- Write, debug and test system firmware before a physical prototype is available.
- Evolve hardware and software design in tandem.
- Diagnostic messages (e.g. illegal instruction) from both CPU and peripheral models detect hard to find programming errors for you.
- Massive productivity gain over traditional embedded design methods. See 'The VSM Advantage' flowchart on page 3, and the testamonial, opposite.

What is Proteus VSM?

Proteus VSM combines mixed mode circuit simulation, animated components and full hardware models of popular micro-controllers. Proteus VSM not only simulates the software running on the micro-controller at the instruction level, but also simulates the on-board peripherals (ADC, USART etc.) right down to waveform level at the device pins. This allows the micro-controller to interact with any analogue or digital electronics connected to it. For example, if the program code writes to a port, the logic levels in the circuit change accordingly and, if the circuit changes the state of the processor's pins, this will be seen by your program code just as in real life.

What can I do with it?

If you are involved in developing any kind of embedded systems, then Proteus VSM will allow you to commence software development before there is a physical prototype to work on.

As well as a particular CPU family, each Proteus VSM package includes models for common peripheral devices such as LCD displays, keypads, buttons, switches and LEDs and you can add your own models to the system too. Consequently you can try out your micro-controller software on a virtual version of your entire product.
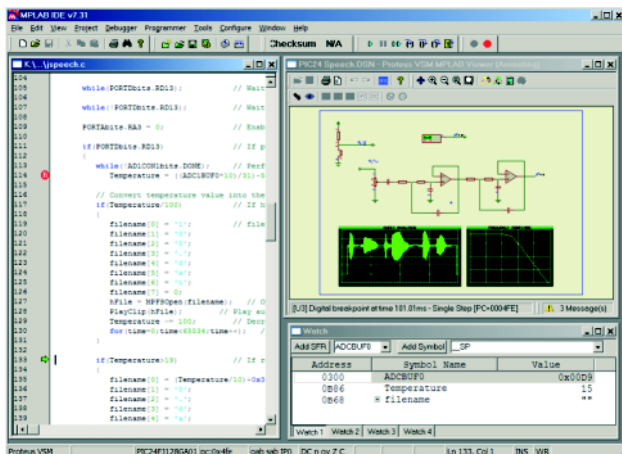
How Accurate are the CPU Models?

Each CPU model is programmed to function as described in the manufacturer's datasheet. This includes instruction execution times, interrupt priorities, interrupt latency, sleep modes and much more. The on-chip peripherals are modelled to a similar level of detail and will generate realistic electrical waveforms at the device pins where appropriate. The models are also subject to extensive

testing using a large number of test-case programs and a conformance mechanism that verifies that the behaviour of the programs is as expected.
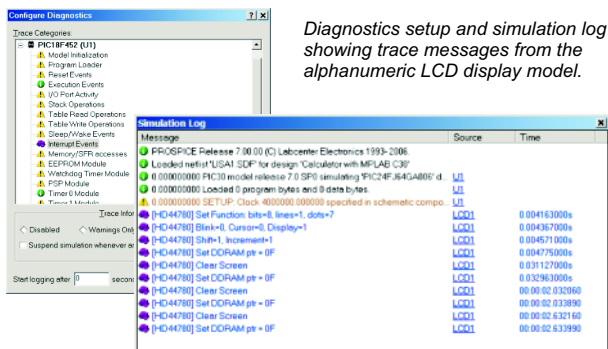
What Debugging Facilities are Provided?

Proteus VSM contains a fully featured built in source level debugger. As you would expect, this features high and low level source code stepping, breakpoints, watch window, memory windows and so on. In addition, you can set breakpoints which will trigger on hardware conditions, and inspect the internal status of external devices (e.g. LCD displays, I2C memories), enabling you to find subtle problems in your designs much more quickly than with conventional tools.

You can also use Proteus VSM in conjunction with selected 3rd party IDEs. For example, the Proteus VSM MPLAB™ Viewer displays your hardware design in a window inside MPLAB and allows you to debug your code exactly as you would on a physical prototype. All the usual debugging features of MPLAB are available including single step, breakpoints, watch window and so on.

Finally, Proteus VSM provides extensive diagnostics from within the device models, allowing you to locate and fix problems in both hardware and software much faster than you could when working on a physical prototype.

Diagnostics setup and simulation log showing trace messages from the alphanumeric LCD display model.

How do I take Measurements?

Proteus VSM comes with a set of virtual instruments including an oscilloscope, logic analyser, signal generators and so on. These allow you to take measurements on your design just as you might with a physical prototype. Better still, we also include master/slave SPI and I2C protocol analysers offering functionality equivalent to very expensive desktop instruments.

What other Devices are Modelled?

The real power of Proteus VSM stems from the fact that you can simulate your firmware as it interacts with a simulation of an entire hardware system. To this end, we provide models for hundreds of common embedded system components including:

- 7-Segment displays, LEDS, lamps and logic indicators.
- Alphanumeric and Graphical LCD displays.
- Universal (i.e. user definable) matrix keypad.
- Buttons, switches and potentiometers.
- Piezo sounder and loudspeaker.
- DC, stepper and servo motor models.
- RAMs, ROMs and I2C EEPROMs.
- Assorted I2C, SPI and 1-Wire I/O expanders and other peripheral devices.
- Storage devices e.g. ATA/IDE hard drive.
- COM port and ethernet physical interface models providing for interaction between the simulation and the real world.

Also, of course, your simulations can make use of any of the 8000 or so standard electronic component models that are included with PROSPICE.

Which Compilers can I Use?

Proteus VSM can simulate the execution of binary files (e.g. HEX) produced by *any* compiler. However, if you wish to single step the high level source code, you need to choose a compiler which can generate one of the supported source level debug formats such as COD, COFF, OMF51, ELF/DWARF, or UBROF.

Alternatively, if you use one of the IDE debug drivers such as the Proteus VSM MPLAB Viewer, then you can use any compiler supported by that IDE.

Please check our website for detailed information about compiler support for each Proteus VSM package.

ARES

Advanced Routing & Editing Software

Our high performance netlist based PCB design software perfectly complements ISIS. Incorporating both automatic component placement and a highly effective rip-up and retry auto-router, ARES transfers both time and effort from you to your PC. On the other hand, if you prefer to route your boards manually, the system places relatively few restrictions on how you go about the task.

PCB Design

Features

- Layers: 16 copper, 2 silk screen, 4 mechanical plus board edge, keepout, resist and solder mask.
- Any angle component placement and pad-stacks.
- Fully automatic ratsnest and force vector generation.
- Drag and Drop pin-swap/gateswap.
- Acclaimed manual routing system is ideal for netlist based manual routing.
- Gridless, polygonal power planes with full control of fill style and thermals.
- Connectivity and physical design rule checkers to prove design integrity.
- Package library includes over 1500 standard footprints.
- Full set of CADCAM output and panelization facilities.
- Pick and Place file for automatic insertion machines.

Design Automation

- Automatic Component Placement.
- Multi-strategy grid based auto-routing
- Special routines for SMT fanouts.
- Rip-Up & Retry for 100% routing on most boards.
- Tidy pass reduces via count and track length.
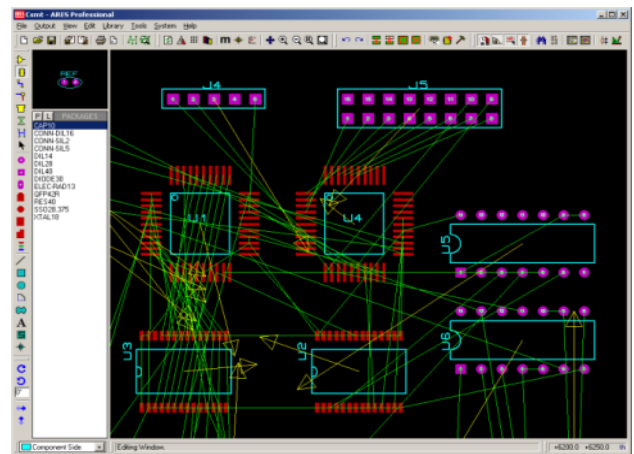- Optional ELECTRA shape-based router available.

Layout Database

ARES features a state of the art layout database capable of representing the most complex of PCB designs. Placement resolution is 10 nanometers within a maximum board size of 20m. Components and other objects may be rotated in 0.1 degree increments whilst padstacks facilitate the achievement of maximum routing area on inner layers.

Netlist & Ratsnest Handling

During the placement phase, ARES displays both the ratsnest and force vectors. Both are updated in real time when you drag components. The ratsnest is also automatically updated during routing - add a track and a ratsnest line will disappear; delete a track and one will re-appear.

The system fully supports design modifications - if you change the schematic and re-load the netlist, ARES will flag up exactly which components and/or tracks are affected. Equally, pin-swaps and gate-swaps made in ARES are automaticaly fed back to the schematic.

Route Placement & Editing

Manual routing makes no requirement that you start from the ratsnest lines (rubberbanding). You can place tracking in any way you wish and ARES will remove ratsnest lines as the connections are actually completed.

When editing routes, you can re-route or delete any section of a track, irrespective of how it was originally placed. Commands are also provided to change the thickness and/or layer of any section of tracking.
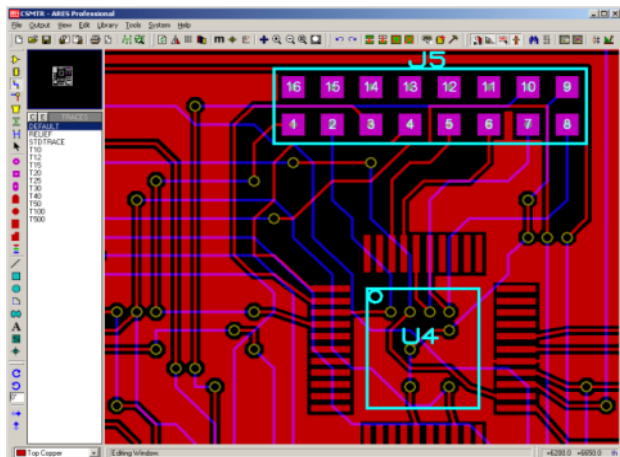
If thick tracks are laid between obstacles such as IC pads, ARES will automatically insert a narrower 'neck' in order to maintain the current design rules.

Curved tracks can be laid down simply by pressing the CTRL key and marking the route with the mouse.

Power Planes

ARES features the ultimate in power plane support - user placeable polygonal regions within which inner boundaries are automatically created around existing pads and tracking. Change the pads and tracking and the boundaries are recomputed to maintain design rule clearances. Thermal reliefs are supported and you can choose whether to hatch or fill each polygon. All computation is based on gridless shape geometry and occurs *in the background* so that you can carry on working on the design.

Design Rule Checks

During manual routing, ARES checks each track as you place it and warns you if any design rules (physical/electrical) are broken via a simple indicator on the status bar. Double click any design rule error and ARES will show you its location on the board.

Package Libraries

The supplied libraries cover a large range of through hole components including all the most common IC, transistor, diode and connector packaging types. We also supply *as standard*, the full IEC libraries for SMT footprints which includes all the standard discrete and IC packaging styles.

New packages can be created directly on the drawing whilst ARES also supports general 2D drafting features.

CADCAM Outputs

As well as providing the basic ability to output your PCB to standard Windows printers, ARES provides an optimized HPGL driver for pen plotters, and a full set of features for professional board manufacturing.

Gerber is supported in both RS274D and the newer RS274X formats whilst a standard Excellon format file is produced for drilling machines. In addition, an ASCII file listing component positions and orientations is produced for use with Pick and Place machinery.
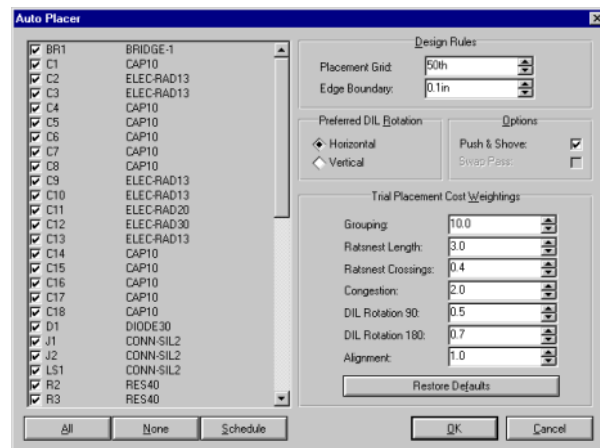
A Gerber Viewer is also provided allowing you to check that Gerber files contain the expected data, and to panelize boards prior to issuing them for manufacture.

Auto-Placement

Automatic component placement makes it possible to design an entire board with the absolute minimum of effort on your part. Alternatively, since the placer can operate interactively, you can pre-place critical components first and the let ARES auto-place the rest.

Auto-Routing

Our grid based router is both flexible and fast and can route using any track thickness or via width, at 90 or 45 degrees, and on 1-8 layers. It was placed in the top Category A in Electronics World's most recent review of PCB software.

The range of routing grids available enables you to trade off routing density against execution speed with densities of 1, 2 or 3 traces between IC pads. The router also has special routines which enable it form 'fan outs' from rows of SMT pads which would otherwise be off grid, thus enabling it to perform well with boards containing SMT parts.

The Rip-Up & Retry mode enables it to remove and replace tracks which block others giving 100% completion on most medium density boards routed at 50 or 25 thou. Meanwhile, our innovative costing/scheduling logic reduces the via count by as much as four fold over other low-medium cost routers.

The built in router also tidy pass which reduces both track length and via count whilst improving the aesthetic quality of your board at the same time.

For those users designing really high density SMT boards, where the built in router may struggle, we also offer the ELECTRA shape based autorouter at substantial discounts. Please see our website for full details of the latest offers.

"PCB design is our business. We review PCB layout software on an ongoing basis and Labcenter has topped the list for the last 10 years. Certainly the most productive and very, very affordable. We have licences for other very expensive products but they don't get much use."

Donald Kay - Don Alan Pty

THE PROTEUS PCB DESIGN PRODUCT RANGE

Proteus PCB Design is available in five levels offering a range of design capacities and features to match your application. Level 1 is limited on both pin count and features whilst Level 2 is limited only in terms of design capacity and offers the full set of features. Level 3 is completely unlimited.

PROSPICE interactive simulation is included with all levels as standard. The Advanced Simulation option which enables the graph based simulation features may be purchased as an optional add-on.

PROTEUS PCB DESIGN	LEVEL 1/1+	LEVEL 2/2+	LEVEL 3
Max Number of Pins in Netlist	1000/2000	1000/2000	Unlimited
Shape based power planes	1 per layer	Unlimited	Unlimited
Standard Auto-routing	✓	✓	✓
Rip-up and Retry Routing		✓	✓
Auto-Placement		✓	✓
Gate-Swap Optimizer		✓	✓

PCB DESIGN LIMITS

PROTEUS Levels 1 and 2 impose a limit for the number of pins in the netlist. These limits apply when loading it into ARES. Any number of pins may be placed on the PCB iteself enabling you to exceed the limit by the odd component should the need arise.

Levels 1+ and 2+ offer double the design capacity but are otherwise identical.

POWER PLANES

All levels of PROTEUS handle power planes using shape based polygon merging. However, in Level 1, only one power plane is allowed per layer - partial power planes and multiple power planes on one layer are supported in Levels 2 and 3 only.

AUTOROUTING

All PROTEUS Levels include a sophisticated multi-strategy autorouter.

In Levels 2 and 3, you also get rip-up and retry operation which will give 100% completion on all but the most complex or densely packed boards.

JUST A FEW OF OUR SATISFIED CUSTOMERS

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Volvo
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British Army SCIAD Branch
Ferrari
British Nuclear Fuels plc
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AMD Automation
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Zetex plc
Assemtech Europe Ltd.
Panasonic
Microchip Technologies
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British Gas plc
Linear Technologies
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Sanyo
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